CLAIMS

1. A semi-conductor device comprising in an integrated way on a substrate:

- a first dynamic threshold voltage MOS transistor (10), with a gate (116), and a channel (111) of a first conductivity type, and

- a current limiter means (20, 30) connected between the gate and the channel of said first MOS transistor,

characterised in that this first MOS transistor is fitted with a first doped zone (160) of the first conductivity type, connected to the channel, and in that the current limiter means comprises a second doped zone (124, 124a) of a second conductivity type, placed against the first doped zone and electrically connected to the first doped zone by an ohmic connection path (180).

2. A device according to claim 1, wherein the current limiter means is a second MOS transistor (20), the second doped zone (124) and a third doped zone (122) of the same conductivity type as the second doped zone forming the source and drain of said second transistor.

3. A device according to claim 2, wherein the second transistor includes a gate (126) connected to a gate polarisation terminal (127).

4. A device according to claim 2, wherein the second transistor (20) has a gate (126) connected to said second doped zone (124).

5. A device according to claim 4, including a terminal (128) in contact with the gate (126) and with the second doped zone (124).

6. A device according to claim 4, wherein the third doped area (122) is connected to the gate (116) of the first MOS transistor (10).

7. A device according to claim 1, wherein the current limiting means is a diode (30), the second doped zone (124a) and a third doped zone (122a), of a conductivity type opposite to that of the second doped zone, forming diode terminals.

8. A device according to claim 7, including a fourth doped zone (121), placed between the second and third doped zones, having the same conductivity type as one of the second and third zones, with a doping concentration lower than that of that zone.

9. A device according to claim 7, wherein the third doped zone (122a) is connected to the gate of the first MOS transistor.

10. A device according to claim 8, wherein the diode comprises a gate (126) extending over the fourth doped zone (121).

11. A device according to claim 10, wherein said diode gate (126) is connected to one of the diode terminals (122a, 124a).

12. A process for manufacturing a device according to claim 2, comprising the following successive stages:

a) preparation in a substrate of an active zone (102), intended to receive the first and second transistors (10, 20) and having a first conductivity type,

b) formation of a first and a second gates (116, 126) above the active zone, corresponding to the first and second transistors respectively, the gates being separated from the substrate by a gate insulator (104) and covering channel areas (111, 121) of the first and second transistors respectively,

c) formation of the first and second source and drain areas (112, 114, 122, 124) of a second conductivity type opposite to the first conductivity type, corresponding to the first and second transistors respectively, by self-aligned ion implantation on the first and second gates, and formation of the first doped zone (160) of the first conductivity type, in contact with the channel (111) of the first transistor, and adjacent to one of the source and drain areas of the second transistor, by self-aligned ion implantation on the gate of the first transistor,

d) formation of a conductive layer (180) in electrical contact with the first doped zone and one of the source and drain areas of the second transistor adjacent to said first doped zone, so as to connect them electrically.

13. A process according to claim 12, including additionally, after stage d) deploying an insulator (183) on the substrate, followed by the formation of

contact points on the source, drain and gate areas of the transistors.

14. A process according to claim 12, including additionally connecting the gate (116) of the first transistor to a doped zone (122) separate from the first doped zone (160) and forming one of the source and drain of the second transistor, and connecting the gate (126) of the second transistor to the first doped zone (160).

15. A process for manufacturing a device according to claim 7, including the following successive stages:

a) preparation in a substrate of a so-called active zone (102) having a first conductivity type, intended to receive the first transistor (101) and the diode (30),

b) formation of a first and a second gates (116, 126) above the active zone, corresponding to the first transistor and to the diode respectively, the gates being separated from the substrate by a gate insulator (104),

c) formation of one of the source and drain areas (112, 114) of the first transistor and of said second doped zone (124a), formation of the first doped zone (160) placed between a channel of the first transistor and the second doped zone, and formation of the third doped zone (122a) separated from the first doped zone by the second doped zone, the source and drain areas and the first doped zone being formed by self-aligned implantations on the first gate,

d) formation of a conductive layer (180) in contact with the first doped zone and the second doped zone, so as to connect them electrically.

16. A process according to claim 15, including additionally, after stage d), deploying an insulator (183) on the substrate, followed by the formation of contact points on the source and drain areas and on the third doped zone.

17. A process according to claim 14, including additionally interconnecting the third doped zone (122a) and the gate (116) of the first transistor.

18. A process according to claim 14, including additionally interconnecting the diode gate (126) and one of the second and third doped zones.

19. A process according to one of claims 12 and 15, wherein stage a) comprises:

- delimiting the active zone according to a field oxidation (LOCOS) or shallow trench isolation technique, and
- doping the active area so as to give it the first conductivity type.

20. A process according to one of claims 12 and 15, wherein the formation of the conductive layer (180) is preceded by the formation of lateral spacers (181) on the gates.

21. A process according to one of claims 12 and 15, wherein the conductive layer (180) is a layer of silicide.